

~~11~~ a first wire, a second wire and a third wire connected to said first source region and drain-region and said first impurity region through contact holes which are so formed as to penetrate said first and second interlayer insulating films and said silicon nitride film, respectively.

~~12~~ Sub B3 7. (Amended) The semiconductor device according to claim 1, wherein said silicon nitride film includes a silicon nitride film entirely formed on said first interlayer insulating film except a portion where contact holes are formed.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8 are pending in the present application. Claims 1-2 and 7 have been amended and Claims 9-14 have been canceled by the present amendment.

In the outstanding Office Action, the drawings were objected; Claims 2 and 7 were objected to; Claims 1-8 were rejected under 35 U.S.C. § 112, second paragraph; and Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art in view of Lou.

Regarding the objection to the drawings, Figures 22-24 are being labeled "Prior Art" as suggested by the examiner. A separate letter requesting approval of these drawing changes is being submitted to the draftsman. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the objections to Claims 2 and 7, the second occurrence of "to" in line 9 of Claim 2 has been deleted. Further, Claim 7 has been amended to recite that the silicon nitride film includes a silicon nitride film entirely formed on the first interlayer insulating film

except a portion where contact holes are formed (see page 21, lines 4-6). Applicants note this further limits the subject matter of independent Claim 1. Accordingly, it is respectfully requested these objections be withdrawn.

Regarding the rejection of Claims 1-8 under 35 U.S.C. § 112, second paragraph, Claims 1 and 2 have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copies. Accordingly, it is respectfully requested this rejection be withdrawn.

Claims 1 and 7 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art in view of Lou. This rejection is respectfully traversed.

The semiconductor device recited in Claim 1 of the present invention includes an SOI substrate having a substrate in which at least its surface is insulative, and a semiconductor layer provided on the surface of the substrate, and an isolation insulating film is formed between first and second active regions both of which are formed in a main surface of said semiconductor layer, leaving a first semiconductor region which is part of the semiconductor layer between itself and the surface of the substrate. Also included is a first interlayer insulating film formed on the first and second active regions and a surface of the isolation insulating film, a silicon nitride film formed on the first interlayer insulating film, and a second interlayer insulating film formed on a surface of the silicon nitride film.

On the other hand, Lou shows in Figure 7 a three-layer structure consisting of an interlayer dielectric layer 210 formed on a substrate 200, a silicon nitride layer 220 formed on the interlayer dielectric layer 210, an intermetal dielectric layer 260 and the like formed on the silicon nitride layer 220. This three-layer structure is similar to a three-layer structure recited in Claim 1 including the first interlayer insulating film, the silicon nitride film and the

second interlayer insulating film in that a silicon nitride film is formed between interlayer insulating films.

However, the three-layer structure of Lou is formed on a bulk substrate 200, whereas the three-layer structure of the present invention is formed on an SOI substrate. Moreover, Lou fails to teach or suggest a structure which corresponds to an isolation insulating film formed on a main surface of a semiconductor layer of an SOI substrate, leaving a first semiconductor region between itself and a surface of a substrate in which at least its surface is insulative, as recited in the present invention.

Further, the present invention recited in Claim 1 realizes a structure including a silicon nitride film on a first interlayer insulating film, so that micro-defects which develop into lifetime killers are generated in the first semiconductor region which is the semiconductor layer below the isolation insulating film by a stress of the silicon nitride film and this shortens the lifetime of carriers.

Consequently, because Lou does not teach or suggest the above-discussed SOI substrate and isolation insulating film of the present invention, one of ordinary skill in the art could not anticipate the present invention recited in Claim 1 for the purpose of shortening the lifetime of carriers in the semiconductor layer below the isolation insulating film, even in consideration of a conventional structure (Figure 22) and disclosure of Lou.

Therefore, because the structure of the present invention and the advantages thereof significantly differ from the combination of Lou with the admitted prior art, it is respectfully submitted Claim 1 and each of the claims depending therefrom are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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Marked-Up Copy
Serial No: 09/729,816
Amendment Filed on:
7-5-02

IN THE CLAIMS

Please cancel Claims 9-14 without prejudice.

--1. (Amended) A semiconductor device comprising:

an SOI substrate [consisting of] including a substrate in which at least its surface is insulative and a semiconductor layer provided on said surface of said substrate, said semiconductor layer having a first active region of a first conductivity type and a second active region of the first conductivity type both of which are provided in a main surface thereof;

an isolation insulating film formed between said first and second active regions in said main surface of said semiconductor layer, leaving a first semiconductor region which is part of said semiconductor layer between [itself] the isolation insulating film and said surface of said substrate;

a first interlayer insulating film formed on said first and second active regions and a surface of said isolation insulating film;

a silicon nitride film formed on said first interlayer insulating film; and

a second interlayer insulating film formed on a surface of said silicon nitride film.

2. (Amended) The semiconductor device according to claim 1, wherein

said substrate includes a semiconductor substrate and a buried insulating film entirely provided on a main surface of said semiconductor substrate,

said semiconductor device further comprising:

first source region and drain region of a second conductivity type formed in said main surface of said semiconductor layer of said first active region [at a predetermined distance] separated from each other;

a first gate electrode so formed on said main surface of said semiconductor layer with a first gate insulating film interposed therebetween as to oppose [to] a region sandwiched between said first source region and drain region;

a first impurity region of the first conductivity type formed in said second active region, being electrically connected to said region sandwiched between said first source region and drain region through said first semiconductor region below said isolation insulating film; and

a first wire, a second wire and a third wire connected to said first source region and drain region and said first impurity region through contact holes which are so formed as to penetrate said first and second interlayer insulating films and said silicon nitride film, respectively.

7. (Amended) The semiconductor device according to claim 1, wherein

said silicon nitride film includes a silicon nitride film entirely formed on said first interlayer insulating film except a portion where contact holes are formed.--